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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,476	01/27/2004	Koji Shimizu	118245	9140
25944	7590	10/16/2007	EXAMINER	
OLIFF & BERRIDGE, PLC			AMADIZ, RODNEY	
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ALEXANDRIA, VA 22320-4850			PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,476	SHIMIZU ET AL.	
	Examiner	Art Unit	
	Rodney Amadiz	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s).

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahan (GB 2,325,329—hereinafter “Ahan”) in view of Haga et al. (USPGPUB 2003/0067434—hereinafter “Haga”) and Watanabe et al. (U.S. Patent 5,534,809—herein referred to as “Watanabe”).

As to **Claim 1**, Ahan teaches an electro-optical device (See Fig. 2), comprising: a plurality of scanning lines (*Pg. 2, line 30 “LCD”—note scanning lines are inherent to LCD’s—see also Fig. 2 and note intersecting dotted lines*); a plurality of data lines (*Fig. 2, DL1, DL2...DL2420*); a plurality of pixels arranged corresponding to intersections between the scanning lines and the data lines to form a matrix (*Fig. 2, note squares in LCD panel 30*).

Examiner cites Ahan to teach a plurality of signal-supplying lines having first ends that are arranged close together and second ends that are arranged close

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together (**Fig. 2, note lines coming out of SWS1, SWS2 and SWS3**); data-line selecting means having a plurality of selecting circuits (**Fig. 2, Reference Numbers 54 and DMP1, DMP2, DMP3, DMP4 and DMP800**) each selecting circuit supplying an image signal to one data line selected from a predetermined number of the data lines on the basis of a plurality of selection signals supplied through the plurality of signal-supplying lines (**Fig. 2, note Image signal outputted from Reference Number 52 and note data lines DL1-DL2400 and Pg. 9, lines 5-30**); a plurality of input terminals provided at the first ends of the plurality of signal-supplying lines (**Fig. 2, note input terminals of SWS1, SWS2 and SWS3**); and selection-signal supplying means for supplying the plurality of selection signals to the first ends and the second ends of the signal-supplying lines (**Fig. 2, note signals SWS1, SWS2 and SWS3—note that although not shown, it is inherent that these signals must come from a device and note that these signals extend to the end, i.e. DMP800**); each of the selecting circuits having a plurality of switching elements (**Fig. 2, Reference Number DMP1—note transistors and Pg. 9, lines 15-23**) and having first input-output terminals connected to the data lines (**Fig. 2, Reference Number DMP1 and data lines DL1, DL2 and DL3 and Pg. 9, lines 15-30**), second input-output terminals connected to a node supplying the image signals (**Fig. 2, Reference Number DMP1 and 52**), and control input terminals to which the selection signals are supplied (**Pg. 9, lines 5-30**); and the plurality of the signal-supplying lines comprising wiring lines from the input terminals to the control input terminals (**Fig. 2—note wiring lines from the input terminals of SWS1, SWS2 and SWS3 to the control input terminals DMP1**). Ahan

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also teaches a plurality of first input terminals provided as the first ends of the plurality of signal-supplying lines (**Fig. 2, note input terminals to SWS1, SWS2 and SWS3**).

Ahan also teaches that a time in which a first switching element among the plurality of switching elements is on is substantially the same time a time in which an adjacent switching element is on (**See Fig. 3 and note switching element times**).

Ahan, however, fails to teach the wiring lines having the same length and width. Examiner cites Watanabe to teach that the concept of having wiring lines of the same length and width is well known (**Col. 6, lines 45-48**). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Watanabe (i.e. make the wiring lines with the same length and width) in the electro-optical device taught by Ahan so that each wire line may be equal in load capacitance (**Col. 6, lines 45-48**).

Ahan also fails to teach a plurality of second input terminals provided as the second ends of the plurality of signal-supplying lines. Examiner cites Haga to teach a second input terminal provided as the second end of the signal-supplying lines (**Fig. 20, Reference Numbers 107 and note that 108 is being fed to both ends of 107—See also Pg. 5, ¶ 80 and Pg. 13, ¶ 218**). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a second input terminal to the signal supplying line as taught by Haga in the electro-optical device taught by Ahan in order to reduce signal delay.

As to **Claim 6**, Ahan teaches an electronic apparatus comprising the electro-optical device of Claim 1 (**See Fig. 2**).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. Patent 7,057,589—hereinafter “Shin”) in view of Watanabe.

As to **Claim 9**, Shin teaches an electro-optical device comprising: scanning lines (**Fig. 4, X1-XM**); data lines (**D1-Dn**); pixels arranged corresponding to intersections between the scanning lines and the data lines to form a matrix (**210 and 212**); signal-supplying lines having first ends that are arranged close together and second ends that are arranged close together (**Fig. 5, 241, 243 and 245; Hr, Hg and Hb**); a selecting circuit (**Fig. 4, 240**) selectively supplying image signals to the data lines on the basis of selection signals supplied through the signal-supplying lines (**See Fig. 5, wherein data signal D1 is supplied to Y1, Y2 and Y3 on the basis of the selection signals (241, 243 and 245) and Col. 7, lines 9-41**), and the selecting circuit including switching elements (**Fig. 5, MR1, MG1 and MB1**) having first input-output terminals connected to the data lines (**Fig. 5, note connection to Y1, Y2 and Y3**), second input-output terminals connected to a node supplying the image signals (**Fig. 5, note connection to D1 through node**), and control input terminals to which the selection signals are supplied (**Fig. 5, note connections from 241, 243 and 245 to MR1, MG1 and MB1, respectively**); and a selection-signal supplying device to supply the selection signals to the first ends of the signal-supplying lines (**Fig. 5, note signals HR, HG and HB coming from controller (not shown)—Col. 7, lines 9-41**), each of the signal-supplying lines including: an input terminal provided as the first end (**Fig. 5, note input terminal to supply the signal-supplying lines with HR, HG and HB—Col. 7, lines 9-41**); a first wiring line extending from the input terminal to the second end (**See lines**

241, 243 and 245); and a second wiring line extending from the first wiring line to the control input terminal (*See lines that connect 241, 243 and 245 to MR1, MG1 and MB1, respectively*).

Shin, however, fails to teach all of the signal-supplying lines having the same width; as well as the length being the same for each signal-supplying line from the first end thereof, through a portion of the first wiring and through the second wiring line, to the control input terminal of the corresponding switching element. Examiner cites Watanabe to teach that the concept of having wiring lines of the same length and width is well known (*Col. 6, lines 45-48*). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Watanabe (i.e. make wiring lines with the same length and width) in the electro-optical device taught by Shin so that each signal-supplying line, from the first terminal to the control input terminal, may be equal in load capacitance (*Col. 6, lines 45-48*).

Response to Arguments

5. Applicant's arguments filed August 1, 2007 have been fully considered but they are not persuasive. As to Claim 1, the Applicant argues the combination of Ahan, Watanabe and Haga to meet the limitations. Specifically, the Applicant states that "a person of ordinary skill in the art would not be motivated to make these lines the same widths and lengths so as to be almost equal in load capacitance to each other, as allegedly taught in Watanabe, because Haga already teaches that the decline in driving

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capability and delay between different gate lines is eliminated. Therefore, a person of ordinary skill in the art would not additionally make the signal line the same width and length." (Pg. 3, last paragraph). The Examiner respectfully disagrees. Watanabe was used to teach that when multiple signal lines have the same length and width they become equal to each other in load capacitance (Col. 6, lines 45-58). Haga, on the other hand, was used to teach that having driver circuits on both ends of line would reduce/eliminate the signal delay between both ends of the lines (§§ 80, 117, 218). It is clearly seen that, having equal load capacitance on signal lines and eliminating signal delays on signal lines are not the same thing. Therefore, the motivation provided is adequate.

As to Claim 9, the Applicant argues that "Shin teaches at col. 10, lines 28-44, that switching elements for recharging are used to solve the problem of resistances of signal lines and gate capacitors causing poor images. Specifically, Shin teaches that the differences in rising time and falling time between switching signals H_1 to H_n are eliminated by generating precharge control signals...a person of ordinary skill in the art would not have been motivated to combine Watanabe with Shine because Shin already provides a solution for the problem the Office Action asserts as providing motivation to combine those references." (Pg. 4, last paragraph). The Examiner respectfully disagrees. In reading Col. 10, lines 28-44, it should be noted that the solution being solved here relates to the RC delay found in the pre-charge circuit due to having a large display. In other words, because the display is so large, it'll take more time to drive the last signal line than it would the first signal line, thereby, limiting the frequency of the

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data driver (Col. 10, lines 34-40). Because the RC delay hinders the data driver the solution provided is to change the precharge according to the RC delay on the signal line by adjusting the precharging switching speed. This is solving a different problem than the one taught by Watanabe, wherein the signal lines with the same length/width are said to have the same load capacitance.

6. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney Amadiz whose telephone number is (571) 272-7762. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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